CLAIMS

[1] A current supply control circuit for controlling an amount of current supplied to a differential circuit, comprising:

a bypass path for bypassing current around said differential circuit;

switching means, interposed in said bypath pass, for opening/closing said bypass path in accordance with a signal level of a clock signal applied from the outside; and

control means for controlling the amount of current supplied to said differential circuit in accordance with the signal level of the clock signal.

[2] The current supply control circuit according to claim 1, wherein said control means adjusts the amount of current in synchronization with opening/closing of said bypass path.

[3] The current supply control circuit according to claim 1 or 2, wherein:

said switching means has a current switching transistor, said transistor having an emitter connected to a common emitter of said differential circuit, and

said control means is connected to a connection point between the emitter of said current switching transistor and the common emitter of said differential circuit.

[4] The current supply control circuit according to claim 3, wherein:

said control means has a current source transistor, said transistor having a collector connected to the connection point, and

said control means further comprises a feedback path for applying

information about the signal level at the collector of said current switching transistor to a base of said current source transistor.

[5] The current supply control circuit according to claim 3, wherein said control means comprises an output terminal for sending the information on the signal level at the collector of said current switching transistor to another logic circuit.

[6] The current supply control circuit according to any of claims 1 to 5, wherein said control means adjusts the current so that the amount of current supplied to said differential circuit when the signal level of the clock signal is at a low level is larger than the amount of current supplied to said differential circuit when the signal level is at a high level.

[7] The current supply control circuit according to any of claims 3 to 6, wherein a parallel circuit comprising of a circuit element having an inductance component and a circuit element having a capacitance element is connected to the collector of said current switching transistor.

[8] The current supply control circuit according to any of claims 3 to 6, wherein a series circuit comprising of a circuit element having an inductance component with a circuit element having a capacitance component is connected to the collector of said current switching transistor.

[9] A latch circuit comprising a first differential circuit for reading a data signal from the outside, a second differential circuit for holding the data

signal, a first current supply control circuit for controlling an amount of current supplied to said first differential circuit, and a second current supply control circuit for controlling the amount of current supplied to said second differential circuit, wherein:

said first current supply control circuit comprises:

a first bypass path for bypassing current around said first differential circuit;

first switching means, interposed in said first bypass path, for opening/closing said first bypass path in accordance with a signal level of a clock signal applied from the outside; and

first control means for controlling the amount of current supplied to said first differential circuit, and

said second current supply control circuit comprises:

a second bypass path for bypassing current around said second differential circuit;

second switching means, interposed in said second bypass path, for opening/closing said second bypass path in accordance with a signal level of a clock complementary signal applied from the outside, said clock complementary signal having a signal level that is the inverse of that of the clock signal; and

second control means for controlling the amount of current supplied to said second differential circuit,

wherein said first control means adjusts the amount of current in accordance with the signal level of the clock signal, and said second control means adjusts the amount of current in accordance with the signal level of the clock complementary signal.

[10] The latch circuit according to claim 9, wherein:

said first switching means has a first current switching transistor, said transistor having an emitter connected to a common emitter of said first differential circuit, and said first control means has a first current source transistor, said transistor having a collector connected to the common emitter of said first differential circuit,

said second switching means has a second current switching transistor, said transistor having an emitter connected to a common emitter of said second differential circuit, and said second control means having a second current source transistor, said transistor having a collector connected to the common emitter of said second differential circuit,

said first current switching transistor has a base connected to a base of said second current source transistor through a first level shift circuit, and

said second current switching transistor has a base connected to the base of said first current source transistor through a second level shift circuit.

[11] The latch circuit according to claim 9, wherein said first and second current supply control circuits are current supply control circuits according to any of claims 1 to 8.

[12] A selector circuit comprising a first differential circuit for reading a first data signal from an outside, a second differential circuit for reading a second data signal from the outside, a first current supply control circuit for controlling an amount of current supplied to said first differential circuit, and a second current supply control circuit for controlling the amount of current

supplied to said second differential circuit, wherein:

said first current supply control circuit comprises:

a first bypass path for bypassing current around said first differential circuit;

first switching means, interposed in said first bypass path, for opening/closing said first bypass path in accordance with a signal level of a clock signal applied thereto from the outside; and

first control means for controlling the amount of current supplied to said first differential circuit, and

said second current supply control circuit comprises:

a second bypass path for bypassing current around said second differential circuit;

second switching means, interposed in said second bypass path, for opening/closing said second bypass path in accordance with a signal level of a clock complementary signal applied from the outside, said clock complementary signal having a signal level that is the inverse of that of the clock signal; and

second control means for controlling the amount of current supplied to said second differential circuit,

wherein said first control means adjusts the amount of current in accordance with the signal level of the clock signal, said second control means adjusts the amount of current in accordance with the signal level of the complementary clock signal, and said selector circuit alternately delivers the first data signal and the second data signal.

[13] The selector circuit according to claim 12, wherein:

said first switching means has s first current switching transistor, said transistor having an emitter connected to a common emitter of said first differential circuit, and said first control means has a first current source transistor, said transistor having a collector connected to the common emitter of said first differential circuit,

said second switching means has a second current switching transistor, said transistor having an emitter connected to a common emitter of said second differential circuit, and said second control means has a second current source transistor, said transistor having a collector connected to the common emitter of said second differential circuit,

said first current switching transistor has a base connected to a base of said second current source transistor through a first level shift circuit, and

said second current switching transistor has a base connected to a base of said first current source transistor through a second level shift circuit.

[14] The selector circuit according to claim 12, wherein said first and second current supply control circuits are current supply control circuits according to any of claims 1 to 8.

[15] A circuit block comprising:

the current supply control circuit according to claim 5; and

a first and a second logic circuit for processing a data signal applied from the outside in synchronization with a change in signal level of a clock signal,

wherein said first logic circuit delivers information about a signal level at a collector of a current switching transistor included in said current supply

control circuit to said second logic circuit as a clock signal.

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